We claim:

Sub B1

1. A square root extraction circuit for calculating binary input data (0.a(1) a(2) a(3) ... a(n)) using a square root extraction algorithm to output binary square root data (0.q(1) q(2) q(3) ... q(m)), said square root extraction algorithm including an algorithm for determining said square root data on the basis of said input data by only additions of square root partial data q(1) to q(m) in q(1) to q(m) order, said square root extraction circuit comprising:

first to *m*th digit calculating portions each including a plurality of adders connected in series so that carries are propagated therethrough, wherein respective ones of said adders which are connected in the last position in said first to *m*th digit calculating portions provide carry outputs serving as said square root partial data q(1) to q(m), respectively, in accordance with said square root extraction algorithm.

2. A square root extraction circuit for calculating binary input data (0.a(1) a(2) a(3) ... a(n)) using a square root extraction algorithm to output binary square root data (0.q(1) q(2) q(3) ... q(m)), said square root extraction algorithm including an algorithm for determining said square root data on the basis of said input data by only additions of square root partial data q(1) to q(m) in q(1) to q(m) order, said algorithm having preceding digit based operation portions for performing operations to output said square root partial data q(2) to q(m) by using said square root partial data q(1) to q(m-1) provided in their preceding digit positions as operation parameters, said square root extraction circuit comprising:

first to *m*th digit calculating portions including at least first to *m*th adder

groups, respectively, each of said first to *m*th adder groups including a plurality of adders connected in series so that carries are propagated therethrough, wherein respective ones of said adders which are connected in the last position in said first to *(p-1)*th digit calculating portions ($2 \leqq p \leqq m$) provide carry outputs serving as said square root partial data q(1) to q(p-1), respectively, in accordance with said square root extraction algorithm, and wherein said preceding digit based operation portions of said *p*th to *m*th digit calculating portions include carry output prediction circuits for performing logic operations based on the carry outputs from respective ones of said adders which are connected in the last position in the adder groups thereof and said square root partial data q(p-1) to q(m-1) provided in their preceding digit positions to output said square root partial data q(p) to q(m), respectively.

3. The square root extraction circuit in accordance with claim 2, further comprising:

a rounding circuit for rounding square root data (0.q(1) q(2) q(3) ...q(k-1)) ($p \leqq k \leqq m$) based on said square root partial data q(k) to q(m) outputted from said carry output prediction circuits of said *k*th to *m*th digit calculating portions to output rounded square root data (0.r(1) r(2) r(3) ... r(k-1)).

4. The square root extraction circuit in accordance with claim 2,

wherein each of said second to *m*th adder groups comprises at least a pair of adders receiving respective external data, and at least a pair of adders each having a first input receiving an addition result from an adder included in an adder group provided in its preceding digit position, said two pairs of adders being

connected in series so that carries are propagated therethrough,

wherein said carry output prediction circuit of said *p*th digit calculating portion performs a logic operation based on addition result information containing information associated with at least an addition result from the adder connected in the last position in the *(p-1)*th adder group in addition to the carry output from the adder connected in the last position in the *p*th adder group and the square root partial data q(p-1) provided in its preceding digit position, thereby to output the square root partial data q(p) and addition result information of the *p*th digit calculating portion, and

wherein said carry output prediction circuit of the *i*th digit calculating portion ($(p+1) \leqq i \leqq m$) performs a logic operation based on an addition result from the adder connected in the last position in the *(i-1)*th adder group and the addition result information of the *(i-1)*th digit calculating portion in addition to the carry output from the adder connected in the last position in the *i*th adder group and the square root partial data q(i-1) provided in its preceding digit position, thereby to output the square root partial data q(i) and addition result information of the *i*th digit calculating portion.

5. The square root extraction circuit in accordance with claim 2,

wherein each of said second to *m*th adder groups comprises at least a pair of adders receiving respective external data, and at least a pair of adders each having a first input receiving an addition result from an adder included in an adder group provided in its preceding digit position, said two pairs of adders being connected in series so that carries are propagated therethrough,

wherein said carry output prediction circuit of said *p*th digit calculating

portion performs a logic operation based on addition result information containing information associated with at least an addition result from the adder connected in the last position in the *(p-1)*th adder group in addition to the carry output from the adder connected in the last position in the *p*th adder group and the square root partial data q(p-1) provided in its preceding digit position, thereby to output the square root partial data q(p) and addition result information of the *p*th digit calculating portion,

wherein said carry output prediction circuit of the *i*th digit calculating portion ((p+1) ≦ i ≦ (m-1)) performs a logic operation based on an addition result from the adder connected in the last position in the *(i-1)*th adder group and the addition result information of the *(i-1)*th digit calculating portion in addition to the carry output from the adder connected in the last position in the *i*th adder group and the square root partial data q(i-1) provided in its preceding digit position, thereby to output the square root partial data q(i) and addition result information of the *i*th digit calculating portion, and

wherein said carry output prediction circuit of the *m*th digit calculating portion performs a logic operation based on an addition result from the adder connected in the last position in the *m*th adder group and the addition result information of the *(m-1)*th digit calculating portion in addition to the carry output from the adder connected in the last position in the *(m-1)*th adder group and the square root partial data q(m-1) provided in its preceding digit position, thereby to output only the square root partial data q(m).

6. The square root extraction circuit in accordance with claim 4,

wherein said carry output prediction circuit of the *i*th digit calculating

portion ((p+1) ≦ i ≦ m) comprises:

logic operation means for performing the logic operation based on the addition result from the adder connected in the last position in the *(i-1)*th adder group and the addition result information of the *(i-1)*th digit calculating portion to output a plurality of logic results; and

selection means for selectively outputting one of said logic results as said square root partial data q(i) and another one of said logic results as the addition result information of the *i*th digit calculating portion on the basis of the carry output from the adder connected in the last position in the *i*th adder group and the square root partial data q(i-1) provided in its preceding digit position.

7. The square root extraction circuit in accordance with claim 6,

wherein said selection means receives the carry output having a negative logic from the adder connected in the last position in the *i*th adder group.

8. The square root extraction circuit in accordance with claim 2,

wherein said square root extraction algorithm includes a step for adding fixed values to be added, and

wherein a fixed addition result is directly applied to an adder in each of said first to *m*th digit calculating portions without using an adder for adding said fixed values.

9. A floating-point square root extraction device for performing a square root extraction operation on floating-point input data including a mantissa and an exponent to output floating-point output data, comprising:

exponent square root extraction means receiving exponent input data for performing the square root extraction operation on said exponent input data to output exponent square root data;

a square root extraction circuit for calculating binary input data associated with mantissa input data (0.a(1) a(2) a(3) ... a(n)) using a square root extraction algorithm to output mantissa square root data (0.q(1) q(2) q(3) ... q(m)), said square root extraction algorithm including an algorithm for determining said mantissa square root data on the basis of said input data by only additions of square root partial data q(1) to q(m) in q(1) to q(m) order, said algorithm having preceding digit based operation portions for performing operations to output said square root partial data q(2) to q(m) by using said square root partial data q(1) to q(m-1) provided in their preceding digit positions as operation parameters,

said square root extraction circuit comprising first to *m*th digit calculating portions including at least first to *m*th adder groups, respectively, each of said first to *m*th adder groups including a plurality of adders connected in series so that carries are propagated therethrough, wherein respective ones of said adders which are connected in the last position in said first to *(p-1)*th digit calculating portions ($2 \leqq p \leqq m$) provide carry outputs serving as said square root partial data q(1) to q(p-1), respectively, in accordance with said square root extraction algorithm, and wherein said preceding digit based operation portions of said *p*th to *m*th digit calculating portions include carry output prediction circuits for performing logic operations based on the carry outputs from respective ones of said adders which are connected in the last position in the adder groups thereof and said square root partial data q(p-1) to q(m-1) provided in their preceding digit positions to output said square root partial data q(p) to q(m), respectively,

said floating-point square root extraction device further comprising

floating-point data output means for outputting said floating-point output data including exponent output data and mantissa output data on the basis of said exponent square root data and said mantissa square root data.

10. The floating-point square root extraction device in accordance with claim 9,

wherein said floating-point data output means includes output selection means receiving input data information indicating whether said floating-point input data is a normalized number or an unnormalized number, said output selection means for forcing said exponent output data to be "0" to output only said mantissa output data as said floating-point output data when said input data information indicates the unnormalized number.

11. The floating-point square root extraction device in accordance with claim 9, further comprising:

data shift means for performing a predetermined data shift processing on said mantissa input data to apply the resultant data as said binary input data to said square root extraction circuit when said exponent input data is an odd number,

wherein said exponent square root extraction means includes:

preliminary exponent square root extraction portion for performing a predetermined change-to-even-number processing on said exponent input data to provide an even number when said exponent input data is an odd number, said preliminary exponent square root extraction portion thereafter dividing the even number by 2 to output preliminary exponent square root data,

said change-to-even-number processing and said predetermined data shift processing being performed so that the value of the floating-point input data is not changed, and

an exponent square root data output portion for modifying said preliminary exponent square root data on the basis of rounding-based carry information to output said exponent square root data, and

wherein said floating-point data output means includes mantissa data rounding means for rounding more significant digits of said mantissa square root data on the basis of a less significant digit of said mantissa square root data to output said mantissa output data and to output said rounding-based carry information indicating whether or not said mantissa square root data has a carry during rounding.

12. The floating-point square root extraction device in accordance with claim 11,

wherein said preliminary exponent square root extraction portion and said exponent square root data output portion are formed integrally.